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10/802,566	03/17/2004	Mou-Shiung Lin	MEG03-002	3507

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EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,566	LIN, MOU-SHIUNG	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/24/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56 and 58-75* is/are pending in the application.

4a) Of the above claim(s) *4, 33-39, 52-54, & 72-75* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-32, 40-51 & 55-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/1/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of embodiment 2 of Figures 3-6 which reads on claims 1-3, 5-32, 40-51 and 55-71 in the reply filed on 7/24/2006 is acknowledged. The traversal is on the ground(s) that the applicant would be forced to bear increased costs if the three species are separately examined; and that the field of search must necessarily cover all species. This is not found persuasive because the fact that species are inter-related does not avoid patentable distinctness among the species. Additionally, the plurality of species makes the examination process unduly burdensome for the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Specification

The disclosure is objected to because of the following informalities:
On page 9, 2nd paragraph, 1st sentence, reference is made to "solder pads 31". On the same page, in the 3rd paragraph, last sentence, solder pads are called out as "solder pads 30" while the solder on the solder pads is referred to as "solder 31". This is confusing.

Appropriate correction is required.

Claim Objections

Claim 49 recites the limitation " said solder pads". There is insufficient antecedent basis for this limitation in the claim or in claim 40 from which claim 49 depends.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 and 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi (US 6,921,980), hereinafter Nakanishi, in view of Liang (US 6,461,895), hereinafter Liang.

Regarding claim 1, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches an integrated circuit chip comprising:

a substrate (2) having semiconductor devices and interconnection lines formed thereover;

a passivation layer (Col. 4, lines 22-24, not shown in figure) overlying said substrate;

a discrete electronic component (8) mounted above said passivation layer; and

one or more wirebonds (12, see Figure 3a) electrically connected to said discrete capacitor (Col. 4, lines 25-28).

However, Nakanishi does not teach that the discrete electronic component is specifically a "capacitor". Liang (refer to Figure 3) teaches that it is well known to use discrete electronic components in conjunction with an integrated circuit chip (12), wherein the discrete electronic component is a capacitor (D-cap), also see (Col. 3, lines 31-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the discrete electronic component is a capacitor. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing de-coupling of noise (see Liang, Col. 1, lines 58-61).

Regarding claim 2, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches said discrete capacitor (8) is connected to said one or more wirebonds (12) through said interconnection (5) lines (Col. 4, lines 25-28).

Regarding claim 3, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches that said one or more wirebonds (12) connect to a contact pad (3) exposed through openings in said passivation layer (Col. 4, lines 22-24, not shown in figure).

Regarding claim 5, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches that the integrated circuit chip further comprises a metal line system (5) overlying said passivation layer.

Regarding claim 6, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches said one or more wirebonds (12) are connected to said capacitor (8) through said metal line (5) system (Col. 4, lines 25-28).

Regarding claim 7, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches that said discrete capacitor (8) is connected to a post-passivation metal line system (5) and wirebonding (12) is also connected to said post-passivation metal line system (Col. 4, lines 25-28).

Regarding claim 8, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches that said discrete capacitor (8) is connected to a post-passivation metal line system (5) and to said wirebonds (12).

Regarding claim 9, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches an integrated circuit chip comprising:

a substrate (2) having semiconductor devices and interconnection lines formed thereover;

a passivation layer (Col. 4, lines 22-24, not shown in figure) overlying said substrate;

a discrete electronic component (8) mounted above said passivation layer; and

one or more wirebonds (12, see Figure 3a) electrically connected to a contact pad (3) formed in openings in said passivation layer.

However, Nakanishi does not teach that the discrete electronic component is specifically a "capacitor". Liang (refer to Figure 3) teaches that it is well known to use discrete electronic components in conjunction with an integrated circuit chip (12), wherein the discrete electronic component is a capacitor (D-cap), also see (Col. 3, lines 31-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the discrete electronic component is a capacitor. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing de-coupling of noise (see Liang, Col. 1, lines 58-61).

Regarding claim 10, Nakanishi (refer to Figure 1b), as modified above, teaches that said capacitor (8) connects to a contact pad (3) formed in openings in said passivation layer (Col. 4, lines 25-28).

Regarding claim 11, Nakanishi (refer to Figure 1b) teaches a post-passivation metal line system (5) overlying said passivation layer (Col. 4, lines 22-24, not shown in figure).

Regarding claim 12, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches that said discrete capacitor (8) is connected to said post-passivation metal line system (5) and to said wirebonds wirebonds (12). Also see Col. 4, lines 25-28.

Regarding claims 68 and 69, Nakanishi (refer to Figure 1b), as modified above, teaches substantially the claimed structure including the said discrete decoupling capacitor (8), but does not specifically disclose that the capacitor is connected to power/ground buses within said substrate. Liang (refer to Figures 1 and 3) teaches a semiconductor device coupled to a discrete capacitor, wherein the capacitor is a decoupling capacitor (Col. 3, lines 30-45) and the capacitor is connected to power/ground buses within a substrate (Col. 5, lines 30-43 & Col. 6, lines 15-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the capacitor is connected to power/ground buses within said substrate. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing decoupling of noise.

Claims 13-14 and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Liang, and further in view of Thomas (US 5,346,858), hereinafter Thomas.

Regarding claims 13 and 66, Nakanishi (refer to Figure 1b) teaches substantially the claimed structure including the said contact pad (3) exposed through said openings in

said passivation layer. However, Nakanishi fails to teach that the said contact pad comprises "an aluminum pad". Thomas teaches a semiconductor device wherein a contact pad comprises an aluminum pad (Col. 2, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the said contact pad comprises an aluminum pad. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a bond pad material with high conductivity which is not as expensive as other high conductivity materials like copper.

Regarding claim 14 and 67, Nakanishi (refer to Figure 1b) teaches substantially the claimed structure including the said contact pad (3) but does not teach that said contact pad comprises "a metal cap" formed in said openings in said passivation layer "on an aluminum pad" underlying said passivation layer. Thomas teaches a semiconductor device wherein a contact pad comprises a metal cap formed in said openings in said passivation layer on an aluminum pad underlying apassivation layer (Col. 2, lines 34-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that said contact pad comprises a metal cap formed in said openings in said passivation layer on an aluminum pad underlying said passivation layer. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a bond pad material with high conductivity with a metal cap that retards corrosion of the pad.

Claims 15, 17-27, 29-32, 40, 42-51, 55, and 58-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Liang, and further in view of Lin (US 6,303,423), hereinafter Lin.

Regarding claim 15, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches an integrated circuit comprising:

semiconductor device structures in and on a substrate (2);

interconnection lines overlying and connecting said semiconductor device structures wherein there is at least one contact pad (3) connected to said interconnection lines;

a passivation layer (Col. 4, lines 22-24, not shown in figure) overlying said interconnection lines;

wirebonds (12, see Figure 3a) formed overlying said passivation layer and connected to said at least one contact pad contact pad (3); and

at least one discrete electronic component (8) mounted on a solder wettable surface (Col. 4, lines 63-67) over said passivation layer.

However, Nakanishi does not specifically teach that the said interconnection lines comprise "a plurality of levels of interconnection lines and interlevel dielectric materials" and that the discrete electronic component is specifically a "discrete decoupling capacitor".

Liang (refer to Figure 3) teaches that it is well known to use discrete electronic components in conjunction with an integrated circuit chip (12), wherein the discrete electronic component is a decoupling capacitor (D-cap), also see (Col. 3, lines 31-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the discrete electronic component is a capacitor. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing de-coupling of noise (see Liang, Col. 1, lines 58-61).

Lin (refer to Figure 1) teaches that it is well known that interconnection lines of an integrated circuit comprise a plurality of levels of interconnection lines (13) and interlevel dielectric materials (14). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the said interconnection lines comprise a plurality of levels of interconnection lines and interlevel dielectric materials. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a large number of interconnects by utilizing multiple layer of interconnects.

Regarding claim 40 and 55, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches a method of fabricating an integrated circuit chip comprising:

forming semiconductor device structures in and on a substrate (2);

forming interconnection lines overlying and connecting said semiconductor device structures wherein a topmost level (i.e. interconnect lines just below the

passivation) of said interconnection lines includes at least one contact pad contact pad (3);

depositing a passivation layer (Col. 4, lines 22-24, not shown in figure) overlying said interconnection lines;

forming first thick metal lines (5) overlying said passivation layer and connecting to said at least one contact pad (3) through openings in said passivation layer;

forming wirebonds (12) on (for claim 40) said first thick metal lines (5) or (for claim 55) said at least one contact pad (3);

forming a solder wettable surface (7, see Col. 4, lines 63-67) on said first thick metal lines (5) adjacent to said wirebonds (12); and

mounting at least one discrete electronic component (8) on said solder wettable surface.

However, Nakanishi does not teach that the said interconnection lines comprise "a plurality of levels of interconnection lines and interlevel dielectric materials" and that the discrete electronic component is specifically a "discrete decoupling capacitor".

Liang (refer to Figure 3) teaches that it is well known to use discrete electronic components in conjunction with an integrated circuit chip (12), wherein the discrete electronic component is a decoupling capacitor (D-cap), also see (Col. 3, lines 31-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the discrete electronic component is a capacitor. The ordinary artisan

would be motivated to modify Nakanishi at least for the purpose of providing de-coupling of noise (see Liang, Col. 1, lines 58-61).

Lin (refer to Figure 1) teaches that it is well known that interconnection lines of an integrated circuit comprise a plurality of levels of interconnection lines (13) and interlevel dielectric materials (14). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the said interconnection lines comprise a plurality of levels of interconnection lines and interlevel dielectric materials. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a large number of interconnects by utilizing multiple layer of interconnects.

Regarding claim 17, Nakanishi teaches said solder wettable surface comprises a printed solder cream (Col. 4, lines 63-67).

Regarding claim 18, Nakanishi teaches that said solder wettable surface comprises solder (Col. 4, lines 63-67).

Regarding claim 19, Nakanishi teaches that a diffusion barrier metal layer (Col. 4, lines 58-62) underlying material having said solder wettable surface.

Regarding claim 20, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches that said at least one decoupling capacitor (8) is connected to said

wirebonds (12) through said contact pad (3) underlying said passivation layer (Col. 4, lines 22-24, not shown in figure).

Regarding claims 21, 51 and 60, Nakanishi as modified above, teaches that said the/at least one discrete decoupling capacitor (8) is connected to (for claim 51) wirebonds (12) and (for claims 21, 51 and 60) to power/ground buses within said substrate (Col. 2, lines 12-27). Liang teaches teaches a semiconductor device coupled to a discrete capacitor, wherein the capacitor is a decoupling capacitor (Col. 3, lines 30-45) and the capacitor is connected to power/ground buses within a substrate (Col. 5, lines 30-43 & Col. 6, lines 15-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the capacitor is connected to power/ground buses within said substrate. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing decoupling of noise.

Regarding claim 22, Nakanishi (refer to Figure 1b) teaches that thick metal lines (5) formed overlying said passivation layer.

Regarding claim 23, Nakanishi (refer to Figure 1b) teaches that said thick metal lines (5) are connected to said contact pad (3) through openings in said passivation layer.

Regarding claim 24, Nakanishi (refer to Figure 1b and 3b), as modified above, teaches that said at least one decoupling capacitor (8) is connected to said wirebonds (12) through said thick metal lines (5). Also see Col. 4, lines 25-28.

Regarding claim 25, Nakanishi (refer to Figure 1b) teaches that said solder wettable surface (7, see Col. 4, lines 63-67) lies on said thick metal lines (5).

Regarding claim 26, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches that said wirebonds (12) are formed on said contact pad (3).

Regarding claim 27, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches that said wirebonds (12) are formed on said thick metal lines (5).

Regarding claim 29, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches the integrated circuit further comprising:

a first post-passivation dielectric layer (4) overlying said passivation layer (Col. 4, lines 22-24, not shown in figure); and

thick metal lines (5) formed overlying said first post-passivation dielectric layer (4) and connected to said contact pad (3) through openings in said first post-passivation dielectric layer and said passivation layer wherein said at least one decoupling capacitor (8) is connected to said wirebonds (12) through said thick metal lines (5).

Regarding claim 30, Nakanishi (refer to Figure 1b) teaches that said first post-passivation dielectric layer (4) comprises polyimide (Col. 4, lines 19-21).

Regarding claim 31, Nakanishi (refer to Figure 1b), as modified above, teaches that the integrated circuit further comprises a second post-passivation dielectric layer (6) overlying said thick metal lines (5) wherein said at least one decoupling capacitor (8) is connected to said thick metal lines (5) through openings in said second post-passivation dielectric layer (6).

Regarding claim 32, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a), as modified above, teaches that the integrated circuit further comprises:

first thick metal lines (5) overlying said passivation layer (Col. 4, lines 22-24, not shown in figure) and connected to said contact pad (3) through openings in said passivation layer;

a first post-passivation dielectric layer (4) overlying said first thick metal lines (5);

a second post-passivation dielectric layer (6) wherein said at least one decoupling capacitor (8) is connected to said wirebonds (12).

However, Nakanishi does not specifically teach a "second thick metal lines". However, the single thick metal line of Nakanishi may be replaced by multiple layers of interconnected thick metal lines by simply repeating the process of the first thick metal line. It would have been obvious to one of ordinary skills in the art at the time of the

invention to form a second thick metals lines overlying said first post-passivation dielectric layer and connected to said first thick metal lines through openings in said first post-passivation dielectric layer such that the second post-passivation dielectric layer is overlying said second thick metal lines and where the said decoupling capacitor is connected to said wirebonds through said second thick metal lines (since wirebonds are connected to the interconnected thick metal lines). The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing more than one layer of thick metal lines, which provide greater flexibility in interconnections.

Regarding claim 42, Nakanishi teaches that the said step of forming said solder wettable surface comprises printing a solder cream on said thick metal lines (Col. 4, lines 63-67).

Regarding claim 43, Nakanishi teaches that said step of forming said solder wettable surface comprises electroless plating said thick metal lines with gold (Col. 4, lines 59-62).

Regarding claim 44, Nakanishi teaches further depositing a diffusion barrier metal layer (Col. 4, lines 58-62) underlying said solder wettable surface and overlying said thick metal lines (5).

Regarding claim 45, Nakanishi (refer to Figure 1b) teaches depositing a first post-passivation dielectric layer (4) overlying said passivation layer and underlying said first thick metal lines (5).

Regarding claim 46, Nakanishi (refer to Figure 1b) teaches said first post-passivation dielectric layer (4) comprises polyimide (Col. 4, lines 19-22).

Regarding claim 47, Nakanishi (refer to Figure 1b) teaches depositing a second post-passivation dielectric layer (6) overlying said first thick metal lines (5).

Regarding claim 48, Nakanishi (refer to Figure 1b) teaches that said second post-passivation dielectric layer (6) comprises polyimide (Col. 3, lines 31-34).

Regarding claim 49, in as much as understood, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches the method further comprising:
depositing a first post-passivation dielectric layer (4) overlying said first thick metal lines (5) and wherein said wirebonds wirebonds (12) and said solder pads (7, see Col. 4, lines 63-67) are formed through openings in said first post-passivation dielectric layer to said first thick metal lines.

Regarding claim 50, Nakanishi (refer to Figure 1b) teaches said first post-passivation dielectric layer (4) comprises polyimide (Col. 4, lines 19-22).

Regarding claim 58, Nakanishi teaches that said step of forming said solder wettable surface comprises printing a solder cream on said first thick metal lines (Col. 4, lines 63-67).

Regarding claim 59, Nakanishi teaches that said step of forming said solder wettable surface comprises electroless plating said first thick metal lines (5) with gold (Col. 4, lines 59-62).

Regarding claim 61, Nakanishi teaches further depositing a diffusion barrier metal layer (Col. 4, lines 58-62) underlying material having said solder wettable surface and overlying said first thick metal lines (5).

Regarding claim 62, Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches the method further comprising: depositing a first post-passivation dielectric layer (4) overlying said passivation layer and underlying said first thick metal lines (5).

Regarding claim 63, Nakanishi (refer to Figure 1b) teaches that said first post-passivation dielectric layer (4) comprises polyimide (Col. 4, lines 19-22).

Regarding claim 64, Nakanishi (refer to Figure 1b) teaches depositing a second post-passivation dielectric layer (6) overlying said first thick metal lines (5).

Regarding claim 65, Nakanishi (refer to Figure 1b) teaches that said second post-passivation dielectric layer (6) comprises polyimide (Col. 3, lines 31-34).

Claims 16, 28, 41 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Liang, further in view of Lin, and still further in view of Murdeshwar (6,267,290), hereinafter Murdeshwar.

Regarding claims 16, 41 and 56, Nakanishi (refer to Figure 3b), as modified above, teaches substantially the claimed structure and method but does not teach that said wirebonds comprise "gold". Murdeshwar teaches wirebonding wherein wirebonds comprise gold (Col. 5, lines 2-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the wirebonds comprise gold. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a wire bond material that is resistant to oxidation (Col. 5, lines 4-6).

Regarding claim 28, Nakanishi (refer to Figure 1b) teaches substantially the claimed structure including a pad (3) that is formed underlying said wirebonds (12) but does not teach that the said pad is a "gold" pad. Murdeshwar teaches wirebonding to a pad, wherein the said pad is a gold pad (Col. 5, lines 2-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the said pad is

a gold pad. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a pad material that is resistant to oxidation (Col. 5, lines 4-6).

Claims 70 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Liang, further in view of Lin, and still further in view of Thomas.

Regarding claim 70, Nakanishi (refer to Figure 1b) teaches substantially the claimed structure including the said contact pad (3) exposed through said openings in said passivation layer, but does not teach that the contact pad comprises "an aluminum pad". Thomas teaches a semiconductor device wherein a contact pad comprises an aluminum pad (Col. 2, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that the said contact pad comprises an aluminum pad. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a bond pad material with high conductivity, which is not as expensive as other high conductivity materials like copper.

Regarding claim 71, Nakanishi (refer to Figure 1b) teaches substantially the claimed structure including the said contact pad (3) and the passivation layer (Col. 4, lines 22-24, not shown in figure) but does not teach that the said contact pad comprises "a metal cap formed in an opening in said passivation layer on an aluminum pad" underlying said passivation layer. Thomas teaches a semiconductor device wherein a contact pad comprises a metal cap formed in said openings in said passivation layer on

an aluminum pad underlying apassivation layer (Col. 2, lines 34-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that said contact pad comprises a metal cap formed in said openings in said passivation layer on an aluminum pad underlying said passivation layer. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a bond pad material with high conductivity with a metal cap that retards corrosion of the pad.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800